Notice of Allowability	Application No.	Applicant(s)	
	10/743,347	KIMURA, HAJIME	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/27/2007*.

2. ☒ The allowed claim(s) is/are *1,3-7,11-23,26,28,29,34,35,40,41,46,47,52,53,62,63,67,68,72,73,77 and 78*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/3/04; 11/7/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

NITIN I. PATEL
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John F. Hayden on 10/18/2007.

Applicant has chose elects Species I, which include claims 1,3-7,11-23,26,28-29,34-35,40-41,46-47,52-53,62-63,67-68,72-73,77-78 and applicant has mad election without traverse, so claims 2,8-10,24-25,27,30-33,36-39,42-45,48-51,54-61,64-66,69-71,74-76,79-85 has been cancelled.

REASON FOR ALLOWANCE

2. Claims 1,3-7,11-23,26,28-29,34-35,40-41,46-47,52-53,62-63,67-68,72-73,77-78 is allowed. Claims 2,8-10,24-25,27,30-33,36-39,42-45,48-51,54-61,64-66,69-71,74-76,79-85 has been cancelled.

3. The following is an examiner's statement of reason for allowance:

Kimura (US 7,193,619) teaches wherein at least one of the current source circuits further comprises a first and second transistors, wherein by a charge accumulated in the capacitor element due to a current supplied when drains and gates of both the first and second transistors is in a short-circuit state a voltage occurring between a gate and a source of one of the first and second transistors is held.

Okabe et al., (US 7154454) shows display device with a driving circuit comprising a selection line for selecting a pixel over which a luminance control is to be carried out, a luminance data line for supplying a voltage corresponding to a luminance, a First transistor which is brought into a conduction state or a non-conduction state in response to a signal of the selection line, a first and second capacitors for holding a voltage from the luminance data line, a second transistor for controlling a current value of a spontaneous light emitting element, a third transistor for connecting or blocking a gate and a drain in the second transistor, a first control signal line for supplying a signal voltage to control the third transistor into a conduction state or a non-conduction state, a fourth transistor for connecting or blocking the spontaneous light emitting element and the second transistor, a second control signal line for supplying a signal voltage to control the fourth transistor into a conduction state or a non-conduction state, and a voltage supply line for supplying a voltage to the spontaneous light emitting element, wherein the device is provided with a switching element capable of short circuiting electrodes of the spontaneous light emitting element.

The prior art fails to teach or suggest a semiconductor device having a first transistor comprising a gate terminal, a first terminal and a second terminal; a second transistor comprising a gate terminal, a first terminal and second terminal; a switch wherein the gate terminal of the first transistor and the first terminal of the first transistor are connected via the switch and means for short-circuiting between the first terminal of the first transistor and the second terminal of the first transistor, wherein the second terminal of the first transistor is connected to the first terminal of the second transistor

and wherein the gate terminal of the first transistor is connected to the gate terminal of the second transistor as claimed in claim 1.

The prior art fails to teach or suggest a switch wherein the gate terminal of the first transistor and the first terminal of the first transistor are connected via the switch and means for short-circuiting between the first terminal of the second transistor and the second terminal of the second transistor, wherein the second terminal of the first transistor is connected to the first terminal of the second transistor and wherein the gate terminal of the first transistor is connected to the gate terminal of the second transistor as claimed in combined limitation of claim 5.

The prior art fails to teach or suggest **a first switch and a second switch wherein the gate terminal of the first transistor and the first terminal of the first transistor are connected via the first switch, wherein the second terminal of the first transistor is connected to the first terminal of the second transistor; wherein the gate terminal of the first transistor is connected to the gate terminal of the second transistor and wherein the first terminal of the second transistor and the second terminal of the second transistor are connected via the second switch** as claimed in combined limitation of claim 6.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

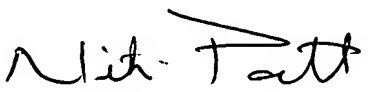
Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Primary Examiner
Art Unit 2629



NITIN I. PATEL
PRIMARY EXAMINER